



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,474	12/01/2003	Masood Murtuza	TI-35639	5891
23494	7590	03/11/2009		
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265				
EXAMINER				
DICKEY, THOMAS L				
ART UNIT		PAPER NUMBER		
2826				
NOTIFICATION DATE		DELIVERY MODE		
03/11/2009		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@ti.com

**Office Action Summary****Application No.**

10/726,474

**Applicant(s)**

MURTUZA, MASOOD

**Examiner**

Thomas L. Dickey

**Art Unit**

2826

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 02 December 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5, 7, 8, 10, 12-14 and 24-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7, 8, 10, 12-14 and 24-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**/Thomas L. Dickey/  
Primary Examiner  
Art Unit 2826**

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

Art Unit: 2826

## DETAILED ACTION

1. The amendment filed on 12/02/2008 has been entered.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 7, 8, 10, 12-14 and 24-33 are rejected under 35 U.S.C. 102(b) as being anticipated by MCTEER (2002/0175362).

With regard to claims 1-5, 7, 8, 10, and 25-28 McTeer discloses a semiconductor device comprising a substrate 12; a plurality of substantially non load bearing inter-level dielectric ILD layers 24, 25 having an ultra low-dielectric material, such as SiLK, FLARE, or Black Diamond (note paragraph 0033 of McTeer) having a dielectric constant (k) between about 1.0 and about 2.7; at least one load bearing support structure 50, 56 (a via formed from a support material comprising aluminum, aluminum alloy, copper, copper alloy, tungsten, or tungsten alloy) disposed in each of the ILD layers 24, 25 at

Art Unit: 2826

locations overlying each other so that support structures 50, 56 are vertically aligned with each other through the plurality of layers; the support column ending at least one additional ILD layer 60 made of AlN and thus having a dielectric constant which is higher than the plurality of ILD layers 24, 25, the at least one additional ILD layer 60 overlying the plurality of ILD layers 24, 25; a contact layer 25a overlying the at least one additional ILD layer 60 and the support structures 50, 56, wherein the at least one additional ILD layer 60 isolates the contact layer 25a from the support structures 50, 56; and a bond pad 56a overlying the contact layer 25a, each of the vertically aligned load bearing support structures 50, 56 substantially aligned with a center axis of the bond pad 56a, so that the support structures 50, 56 are located underneath a bond pad 56a location (the bond pad 56a location being the nominal "source of the stress") , wherein the at least one support structure 50, 56 is a plurality of support structures 50, 56, the semiconductor device further comprising a solder bump overlying the contact surface, the plurality of support structures 50, 56 being located directly underneath the solder bump and the at least one support structure 50, 56 is a plurality of support structures 50, 56, the semiconductor device further comprising a solder bump overlying the contact surface, the plurality of support structures 50, 56 being located directly underneath the solder bump. Note figure 10 and paragraphs 0031-0044 of McTeer.

Art Unit: 2826

The applicant's claims 1-5, 7, 8, 10, and 25-28 do not distinguish over the McTeer reference regardless of the claims reciting the performing of certain function(s) using the claimed device, because only the device per se is relevant, not the recited functions of using the support structures for mitigating damage to the semiconductor device and mitigating structural damage of the plurality of ILD layers caused by stresses to the plurality of ILD layers due to forces applied onto the plurality of ILD layers 24, 25 during one of a subsequent processing and packaging of the semiconductor device.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir. 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); *Ex parte Smith*, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are

Art Unit: 2826

produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"); *Ex parte* THOMAS J. WHALEN II, slip opinion<sup>1</sup>, page 13, (BPAI, PRECEDENTIAL, decided July 23, 2008) ("[T]he examiner must provide some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art' before the burden is shifted to the applicant to disprove the inherency"); and *Leggett & Platt Inc. v. VUTEk Inc.*, 537 F3d 1349, 1352, 87 USPQ2d 1947, 1951 (Fed. Cir. 2008) ("Moreover, because the claim is written with functional rather than structural language—it requires the cold UV assembly to be 'effective to' substantially cure rather than requiring ink to be substantially cured—the claim limitation will be anticipated so long as the LEDs disclosed in the '823 patent are able to cure the ink to a great extent"). See MPEP § 2114.

In this case, it is reasonable to predict that McTeer's device is capable of using the support structures for mitigating damage to the semiconductor device and mitigating structural damage of the plurality of ILD layers caused by stresses to the plurality of ILD layers due to forces applied onto the plurality of ILD layers 24, 25 during one of a subsequent processing and packaging of the semiconductor device, because a

---

<sup>1</sup> Available at the BPAI website as <http://www.uspto.gov/web/offices/dcom/bpai/prec/fd074423.pdf>

Art Unit: 2826

comparison of Applicant's specification to McTeer's disclosure reveals that McTeer discloses a device that is apparently identical to the device Applicant describes as being capable of performing the function(s) of using the support structures for mitigating damage to the semiconductor device and mitigating structural damage of the plurality of ILD layers caused by stresses to the plurality of ILD layers due to forces applied onto the plurality of ILD layers 24, 25 during one of a subsequent processing and packaging of the semiconductor device.

Because it is reasonable to predict that assume that McTeer's device is capable of performing the claimed function, the burden shifts to Applicants to come forward with evidence showing that the prior art device, despite reasonable appearances, is not so capable. See MPEP § 2114.

With regard to claims 12, 13, 29, and 30 McTeer discloses a semiconductor device comprising a substrate 12; a plurality of substantially non load bearing inter-level dielectric inter-level dielectric ILD layers 24, 25 having a dielectric material, such as SiLK, FLARE, or Black Diamond (note paragraph 0033 of McTeer) having a dielectric constant (k) between about 1.0 and about 3.8; a plurality of load bearing support structures 50, 56 disposed in each of the ILD layers 24, 25 at locations overlying each other so that support structures 50, 56 are vertically aligned with each other through the plurality of layers; at least one additional ILD layer 60 made of AlN and thus having a

Art Unit: 2826

dielectric constant<sup>2</sup> which is higher than the plurality of ILD layers 24, 25, the at least one additional ILD layer overlying the plurality of ILD layers 24, 25; a contact layer 25a overlying the at least one additional ILD layer 60 and the support structures 50, 56, wherein the at least one additional ILD layer 60 isolates the contact layer 25a from the support structures 50, 56; wherein a plurality of support structures 50, 56 are disposed in the at least one of the plurality of dielectric layers in an  $n \times m$  matrix configuration, where  $n$  and  $m$  are integers greater than one (note paragraph 0041 of McTeer); and wherein each of the plurality of support structures 50, 56 of each matrix configuration are disposed at a location vertically aligned and the matrix configurations are uniformly distributed below and corresponding to a size of a bond pad 56a disposed on the semiconductor device, wherein the plurality of support structures are disposed in the plurality of ILD layers at a plurality of locations spaced equidistant apart from each other across substantially the entirety of each of the plurality of ILD layers, and the  $n \times m$  plurality of support structures are configured such that the  $n$  support structures extend along a length of the semiconductor device and the  $m$  support structures extend along a width of the semiconductor device, the plurality  $n$  support structures and the plurality

---

<sup>2</sup> The dielectric constant of AlN is well known in the art to be about 9. See, e.g., paragraph 0540 of Kirkpatrick et al. 2002/0167282.



Art Unit: 2826

m support structures intersecting perpendicularly with respect to each other. Note figure 10 and paragraphs 0031-0044 of McTeer.

The applicant's claims 12, 13, 29, and 30 do not distinguish over the McTeer reference regardless of the claims reciting the performing of certain function(s) using the claimed device, because only the device per se is regardless of the claims reciting the performing of certain function(s) using the claimed device, because only the device per se is relevant, not the recited functions of stressing the plurality of ILD layers and mitigating structural damage of the plurality of ILD layers.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in original]); *In re King*, 231 USPQ 136 (Fed. Cir. 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); *Ex parte Smith*, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) ("Where, as here,

Art Unit: 2826

the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"); *Ex parte* THOMAS J. WHALEN II, slip opinion, page 13, (BPAI, PRECEDENTIAL, decided July 23, 2008) ("[T]he examiner must provide some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art' before the burden is shifted to the applicant to disprove the inherency"); and *Leggett & Platt Inc. v. VUTEk Inc.*, 537 F3d 1349, 1352, 87 USPQ2d 1947, 1951 (Fed. Cir. 2008) ("Moreover, because the claim is written with functional rather than structural language—it requires the cold UV assembly to be 'effective to' substantially cure rather than requiring ink to be substantially cured—the claim limitation will be anticipated so long as the LEDs disclosed in the '823 patent are able to cure the ink to a great extent"). See MPEP § 2114.

In this case, it is reasonable to predict that McTeer's device is capable of mitigating structural damage of the plurality of ILD layers caused by stresses to the plurality of ILD layers, because a comparison of Applicant's specification to McTeer's disclosure reveals that McTeer discloses a device that is apparently identical to the device Applicant describes as being capable of performing the function(s) of mitigating

Art Unit: 2826

structural damage of the plurality of ILD layers caused by stresses to the plurality of ILD layers.

Because it is reasonable to predict that assume that McTeer's device is capable of performing the claimed function, the burden shifts to Applicants to come forward with evidence showing that the prior art device, despite reasonable appearances, is not so capable. See MPEP § 2114.

With regard to claims 24 and 31-33 McTeer discloses a semiconductor device comprising a substrate 12; a plurality of substantially non load bearing inter-level dielectric ILD layers 24, 25 each formed of a dielectric material, such as SiLK, FLARE, or Black Diamond (note paragraph 0033 of McTeer) having a dielectric constant (k) between about 1.0 and about 3.8; at least one load bearing support structure 50, 56 disposed in each of the ILD layers 24, 25 at locations overlying each other so that support structures 50, 56 are vertically aligned with each other through the plurality of layers; at least one additional ILD layer 60 made of AlN and thus having a dielectric constant which is higher than the plurality of ILD layers 24, 25, the at least one additional ILD layer 60 overlying the plurality of ILD layers 24, 25; a bond pad 56a overlying the at least one additional ILD layer 60 and the support structures 50, 56, wherein the at least one support structure 50, 56 is a plurality of support structures 50, 56, the plurality of vertically aligned load bearing support structures 50, 56 being located

Art Unit: 2826

directly underneath the bond pad 56a and substantially aligned with a center axis of the bond pad 56a, wherein the at least one support structure 50, 56 comprises a first plurality of support structures 50, 56 extending along a length of the semiconductor device and a second plurality of support structures 50, 56 extending along a width of the semiconductor device, the first and second plurality of support structures 50, 56 intersecting perpendicularly with respect to each other, wherein the at least one support structure 50, 56 comprises a first plurality of support structures 50, 56 extending along a length of the semiconductor device and a second plurality of support structures 50, 56 extending along a width of the semiconductor device, the first and second plurality of support structures 50, 56 intersecting perpendicularly with respect to each other. Note figure 10 and paragraphs 0031-0044 of McTeer.

The applicant's claims 24 and 31-33 do not distinguish over the McTeer reference regardless of the claims reciting the performing of certain function(s) using the claimed device, because only the device per se is relevant, not the recited functions of stressing the plurality of ILD layers and mitigating structural damage of the plurality of ILD layers.

Note that functional language in a device claim is directed to the device per se, no matter which of the device's functions is referred to in the claim. *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) ("[A]pparatus claims cover what a device *is*, not what a device *does*" [emphasis in

Art Unit: 2826

original]]; *In re King*, 231 USPQ 136 (Fed. Cir, 1986) ("It did not suffice merely to assert that [the cited prior art] does not inherently achieve [the claimed function], challenging the PTO to prove the contrary by experiment or otherwise. The PTO is not equipped to perform such tasks"); *In re Best*, 562 F.2d 1252, 1254, 195 USPQ 430, 433 (CCPA 1977) (claiming a new use, new function or unknown property which is inherently present in the prior art does not necessarily make the claim patentable); *Ex parte Smith*, 83 USPQ2d 1509, 1514 (Bd. Pat. App. & Int. 2007, PRECEDENTIAL) ("Where, as here, the claimed and prior art products are identical or substantially identical, or are produced by identical or substantially identical processes, the PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product"); *Ex parte THOMAS J. WHALEN II*, slip opinion, page 13, (BPAI, PRECEDENTIAL, decided July 23, 2008) ("[T]he examiner must provide some evidence or scientific reasoning to establish the reasonableness of the examiner's belief that the functional limitation is an inherent characteristic of the prior art' before the burden is shifted to the applicant to disprove the inherency"); and *Leggett & Platt Inc. v. VUTEk Inc.*, 537 F3d 1349, 1352, 87 USPQ2d 1947, 1951 (Fed. Cir. 2008) ("Moreover, because the claim is written with functional rather than structural language—it requires the cold UV assembly to be 'effective to' substantially cure rather than requiring ink to be substantially cured—the claim limitation will be anticipated so

Art Unit: 2826

long as the LEDs disclosed in the '823 patent are able to cure the ink to a great extent"). See MPEP § 2114.

In this case, it is reasonable to predict that McTeer's device is capable of mitigating structural damage of the plurality of ILD layers caused by stresses to the plurality of ILD layers, because a comparison of Applicant's specification to McTeer's disclosure reveals that McTeer discloses a device that is apparently identical to the device Applicant describes as being capable of performing the function(s) of mitigating structural damage of the plurality of ILD layers caused by stresses to the plurality of ILD layers.

Because it is reasonable to predict that assume that McTeer's device is capable of performing the claimed function, the burden shifts to Applicants to come forward with evidence showing that the prior art device, despite reasonable appearances, is not so capable. See MPEP § 2114.

#### ***Response to Arguments***

4. Applicant's arguments with respect to claims 1-5, 7, 8, 10, 12-14 and 24-33 have been considered but are moot in view of the new ground(s) of rejection.

Art Unit: 2826

***Conclusion***

**5. THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent

Art Unit: 2826

Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

***/Thomas L. Dickey/  
Primary Examiner  
Art Unit 2826***